OMKAR PATHAK
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EDUCATION:

University of Southern California, Los Angeles
Master of Sciences: Electrical Engineering (VLSI) May 2013
GPA for first semester 3.7

Government College of Engineering, Aurangabad, India
Bachelor of Engineering
Department: Electronics and Telecommunication June 2011
GPA for B.E. 8.1 / 10

TECHNICAL SKILLS:

Programming Languages: Verilog, Xilinx VHDL, C
Applications: MS office, Cadence, LTspice, MATLAB

COURSE LIST FALL 2011:

EE-477L – Digital CMOS Integrated Circuits
EE- 457 – Computer Organization
EE- 479 – Analysis of Analog CMOS Integrated Circuits

PROJECT EXPERIENCE:

Design of a synchronous two directional timer (successfully implemented using Cadence)
Aim: To design a synchronous two directional timer to achieve minimum area-delay product using tsmc 180nm
-Designed the schematic and layout in cadence virtuoso and used spectre for simulation
-Minimized delay using carry look-ahead technique in design of datapath

Design of an Operational Amplifier (successfully implemented using LTspice)
Aim: To Design a two stage operational amplifier using IBM 65nm technology
-Designed a PTAT current source for the OPAMP with very high PSRR
-Designed folded cascode as an input stage and common source as an output stage of the opamp
-Specifications achieved gain 112dB, settling time 5.5ns, phase margin 70 degrees and gain bandwidth 1.123 GHz

Design of a simple five stage pipeline (successfully implemented using Modelsim)
-Pipeline could support ADD4, SUB3 & MOV instructions
-ADD4 and SUB3 could add integer 4 and subtract integer 3 to a source register
-Implemented the pipeline in RTL coding using Modelsim
-Modified the pipeline from five stage to four stage and observed how the performance changes

Measurement and representation of temperature profile of chemical (successfully completed using VB)
Aim: To achieve a cost effective technique for determining melting/boiling point of chemical
-Used Visual Basic for image processing avoiding MATLAB